**BPU Question 1**

Considering a 2-bit saturating counter BHT of 1K entries; and assuming that the processor executes the following code fragment, determine the BHT final state and calculate the misprediction ratio in the presented case. The BPU initial state is indicated in the table.

General assumptions:

* R10 is the main loop control register and is initialized to 100
* R3 and R7 are reference values set to 5
* R2 and R6 are input registers
  + R2 input values are always higher than 5
  + R6 input values are always lower than 5

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Address** | **Instruction** | | **BHT (2-bit)** | **Prediction** | **misP. counter** |
| **0x0000** | **L0:** | **…** | **0** | **NT** |  |
| **…** | ; | ***Reading input values*** | **0** | **NT** |  |
| **0x0010** |  | **SLT R1, R2, R3** | **0** | **NT** |  |
| **0x0014** |  | **BEQZ R1, L1** | **0** | **NT** |  |
| **0x0018** |  | **DADDI R2, R0, 10** | **0** | **NT** |  |
| **0x001C** | **L1:** | **SLT R4, R6, R7** | **0** | **NT** |  |
| **0x0020** |  | **BEQZ R4, L2** | **0** | **NT** |  |
| **0x0024** |  | **DADDI R12, R0, 10** | **0** | **NT** |  |
| **0x0028** | **L2:** | **DSUB R3, R1, R2** | **0** | **NT** |  |
| **0x002C** |  | **BEQZ R3, L3** | **0** | **NT** |  |
| **0x0030** |  | **…** | **0** | **NT** |  |
| **0x0038** | **L3:** | **…** | **0** | **NT** |  |
| **0x003c** |  | **DADDI R10, R10, #-1** | **0** | **NT** |  |
| **0x0040** |  | **BNEZ R10, L0** | **0** | **NT** |  |
| **0x0044** |  | **…** | **0** | **NT** |  |

Note:

SLT R1,R2,R3 ;IF (R2 < R3) R1 🡨 1

;ELSE R1 🡨 0

**BPU Question 2**

Considering a (2,2) correlating predictor of 1K entries; and assuming that the processor executes the following code fragment, determine the BPU final state and calculate the misprediction in the presented case. The BPU initial state is indicated in the table.

General assumptions:

* R10 is the main loop control register and is initialized to 100
* R3 and R7 are reference values set to 5
* R2 and R6 are input registers
  + R2 input values are always higher than 5
  + R6 input values are always lower than 5

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Address** | **Instruction** | | **2-bit predictors** | | | | **2-bit shift register** | | **misP. counter** |
| **00** | **01** | **10** | **11** |
| **0x0000** | **L0:** | **…** | **0** | **0** | **0** | **0** | **00** | |  |
| **…** | ; | ***Reading input values*** | **0** | **0** | **0** | **0** | **init** | **end** |  |
| **0x0010** |  | **SLT R1, R2, R3** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0014** |  | **BEQZ R1, L1** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0018** |  | **DADDI R2, R0, 10** | **0** | **0** | **0** | **0** |  |  |  |
| **0x001C** | **L1:** | **SLT R4, R6, R7** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0020** |  | **BEQZ R4, L2** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0024** |  | **DADDI R12, R0, 10** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0028** | **L2:** | **DSUB R3, R1, R4** | **0** | **0** | **0** | **0** |  |  |  |
| **0x002C** |  | **BEQZ R3, L3** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0030** |  | **…** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0038** | **L3:** | **…** | **0** | **0** | **0** | **0** |  |  |  |
| **0x003c** |  | **DADDI R10, R10, #-1** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0040** |  | **BNEZ R10, L0** | **0** | **0** | **0** | **0** |  |  |  |
| **0x0044** |  | **…** | **0** | **0** | **0** | **0** |  |  |  |